

CLAIMS

What is claimed is:

1 1. A microelectronic substrate, comprising:
2 a first microelectronic substrate core having a first surface and an opposing
3 second surface, said first microelectronic substrate core having at least one opening
4 defined therein extending from said first microelectronic substrate core first surface to
5 said first microelectronic substrate core second surface;
6 at least one first microelectronic device disposed within said at least one opening,
7 said at least one first microelectronic device having an active surface and a back surface,
8 wherein said first microelectronic device active surface is adjacent said first
9 microelectronic substrate core first surface;
10 an encapsulation material adhering said first microelectronic substrate core to said
11 at least one first microelectronic device forming a first surface adjacent said
12 microelectronic die active surface and said core first surface and a second surface
13 adjacent said microelectronic die back surface and said core second surface; and
14 at least one conductive vià extending from said first microelectronic substrate
15 core first surface to said first microelectronic substrate core second surface.

1 2. The microelectronic substrate of claim 1, further including a first
2 interconnection layer disposed proximate said first microelectronic substrate core first
3 surface and said first microelectronic device active surface and further including a second
4 interconnection layer disposed proximate said first microelectronic substrate core second

5 surface and said first microelectronic device back surface, wherein said at least one
6 conductive via electrically connects said first interconnection layer and said second
7 interconnection layer.

1 3. The microelectronic substrate of claim 2, further including at least one
2 microelectronic device attached to at least one of said first interconnection layer and said
3 second interconnection layers.

1 4. The microelectronic substrate of claim 2, further including at least one
2 heat dissipation device thermally attached to said at least one microelectronic device back
3 surface.

1 5. The microelectronic substrate of claim 2, wherein said first
2 interconnection layer comprises at least one dielectric layer abutting at least one of said
3 first microelectronic device active surface, said first microelectronic substrate core first
4 surface, and said encapsulation material first surface, and at least one conductive trace
5 disposed on said at least one dielectric layer.

1 6. The microelectronic substrate of claim 5, wherein said at least one
2 conductive trace extends through said at least one dielectric layer to contact at least one
3 electrical contact on said first microelectronic device active surface.

1 7. The microelectronic substrate of claim 5, wherein said at least one
2 conductive trace extends through said at least one dielectric layer to contact said at least
3 one conductive via.

1 8. The microelectronic substrate of claim 2, wherein said second
2 interconnection layer comprises at least one dielectric layer abutting at least one of said
3 microelectronic device back surface, said microelectronic substrate core second surface,
4 and said encapsulant material second surface, and at least one conductive trace disposed
5 on said at least one dielectric layer.

1 9. The microelectronic substrate of claim 8, wherein said at least one
2 conductive trace extends through said at least one dielectric layer to contact said at least
3 one conductive via.

1 10. The microelectronic substrate of claim 1, further including:
2 a second microelectronic substrate core having a first surface and an opposing
3 second surface, said second microelectronic substrate core having at least one opening
4 defined therein extending from said second microelectronic substrate core first surface to
5 said second microelectronic substrate core second surface;
6 at least one second microelectronic device disposed within said at least one
7 opening, said at least one second microelectronic device having an active surface

8 adjacent said second microelectronic substrate core first surface and a back surface
9 adjacent said second microelectronic substrate core second surface;
10 an encapsulation material adhering said second microelectronic substrate core to
11 said at least one second microelectronic device forming a first surface adjacent said
12 microelectronic die active surface and said core first surface and a second surface
13 adjacent said microelectronic die back surface and said core second surface;
14 said first microelectronic substrate core second surface attached to said second
15 microelectronic substrate core second surface; and
16 said at least one conductive via extends from said first microelectronic substrate
17 core first surface to said second microelectronic substrate core first surface.

1 11. The microelectronic substrate of claim 10, further including a heat
2 dissipation device disposed between said first microelectronic substrate core second
3 surface and said second microelectronic substrate core second surface.

1 12. The microelectronic substrate of claim 11, further including a dielectric
2 material disposed between said conductive via and said heat dissipation device.

1 13. A microelectronic substrate, comprising:
2 at least one first microelectronic device having an active surface and a back
3 surface;

4 an encapsulation material forming a first surface adjacent said microelectronic die
5 active surface and a second surface adjacent said microelectronic die back surface; and
6 at least one conductive via extending from said encapsulation material first
7 surface to said encapsulation material second surface.

1 14. The microelectronic substrate of claim 13, further including a first
2 interconnection layer disposed proximate said encapsulation material first surface and
3 said first microelectronic device active surface and further including a second
4 interconnection layer disposed proximate said encapsulation material second surface and
5 said first microelectronic device back surface, wherein said at least one conductive via
6 electrically connects said first interconnection layer and said second interconnection
7 layer.

1 15. A microelectronic substrate, comprising:
2 a first microelectronic substrate core having a first surface and an opposing
3 second surface, said first microelectronic substrate core having at least one opening
4 defined therein extending from said first microelectronic substrate core first surface to
5 said first microelectronic substrate core second surface;
6 at least one first microelectronic device disposed within said at least one opening,
7 said at least one first microelectronic device having an active surface and a back surface,
8 wherein said first microelectronic device active surface is adjacent said first
9 microelectronic substrate core first surface;

10 a first encapsulation material adhering said first microelectronic substrate core to
11 said at least one first microelectronic device forming a first surface adjacent said
12 microelectronic die active surface and said core first surface and a second surface
13 adjacent said microelectronic die back surface and said core second surface;
14 a second microelectronic substrate core having a first surface and an opposing
15 second surface, said second microelectronic substrate core having at least one opening
16 defined therein extending from said second microelectronic substrate core first surface to
17 said second microelectronic substrate core second surface;
18 at least one second microelectronic device disposed within said at least one
19 opening, said at least one second microelectronic device having an active surface and a
20 back surface, wherein said second microelectronic device active surface is adjacent said
21 second microelectronic substrate core first surface;
22 a second encapsulation material adhering said second microelectronic substrate
23 core to said at least one second microelectronic device forming a first surface adjacent
24 said microelectronic die active surface and said core first surface and a second surface
25 adjacent said microelectronic die back surface and said core second surface; and
26 said first microelectronic device active surface oriented to face said second
27 microelectronic device active surface.

1 16. The microelectronic substrate of claim 15, further including a first
2 interconnection layer disposed proximate said first microelectronic substrate core first
3 surface, said first encapsulation first surface, and said first microelectronic device active

4 surface and further including a second interconnection layer disposed proximate said
5 second microelectronic substrate core first surface, said second encapsulation material
6 first surface, and said first microelectronic device active surface, wherein said first and
7 second interconnection layers are electrically connected.

1 17. The microelectronic substrate of claim 15, further including an
2 interconnection layer disposed proximate at least one of said first microelectronic
3 substrate core second surface, said first encapsulation material second surface, and said
4 first microelectronic device back surface, and said second microelectronic substrate core
5 second surface, said second encapsulation material second surface, and said second
6 microelectronic device back surface.

1 18. The microelectronic substrate of claim 15, further including at least one
2 conductive via extending from said first microelectronic substrate core first surface and
3 said first microelectronic substrate core second surface.

1 19. The microelectronic substrate of claim 15, further including at least one
2 conductive via extending between said second microelectronic substrate core first surface
3 and said second microelectronic substrate core second surface.

1 20. The microelectronic substrate of claim 15, further including at least one
2 conductive via extending from said first microelectronic substrate core second surface
3 and said second microelectronic substrate core second surface.

1 21. The microelectronic substrate of claim 15, further including at least one
2 heat dissipation device thermally attached to at least one of said at least one first
3 microelectronic device back surface and said at least one second microelectronic device
4 back surface.

1 22. A microelectronic substrate, comprising:
2 a first microelectronic substrate core having a first surface and an opposing
3 second surface, said first microelectronic substrate core having at least one cavity defined
4 therein;
5 at least one first microelectronic device disposed within said at least one cavity,
6 said at least one first microelectronic device having an active surface and a back surface,
7 wherein said first microelectronic device active surface is adjacent said first
8 microelectronic substrate core first surface;
9 a first encapsulation material adhering said first microelectronic substrate core to
10 said at least one first microelectronic device forming a first surface adjacent said
11 microelectronic die active surface;

12 a second microelectronic substrate core having a first surface and an opposing
13 second surface, said second microelectronic substrate core having at least one cavity
14 defined therein;
15 at least one second microelectronic device disposed within said at least one
16 cavity, said at least one second microelectronic device having an active surface and a
17 back surface, wherein said second microelectronic device active surface is adjacent said
18 second microelectronic substrate core first surface;
19 a second encapsulation material adhering said second microelectronic substrate
20 core to said at least one second microelectronic device forming a first surface adjacent
21 said microelectronic die active surface and said core first surface; and
22 said first microelectronic device active surface oriented to face said second
23 microelectronic device active surface.

1 23. The microelectronic substrate of claim 22, further including a first
2 interconnection layer disposed proximate said first microelectronic substrate core first
3 surface, said first encapsulation first surface, and said first microelectronic device active
4 surface and further including a second interconnection layer disposed proximate said
5 second microelectronic substrate core first surface, said second encapsulation material
6 first surface, and said first microelectronic device active surface, wherein said first and
7 second interconnection layers are electrically connected.

1 24. A method of fabricating a microelectronic substrate, comprising:

2 providing a first microelectronic substrate core having a first surface and an
3 opposing second surface, said first microelectronic substrate core having at least one
4 opening defined therein extending from said first microelectronic substrate core first
5 surface to said first microelectronic substrate core second surface;
6 disposing at least one first microelectronic device having an active surface and a
7 back surface within said at least one opening such that said first microelectronic device
8 active surface resides adjacent said first microelectronic substrate core first surface;
9 disposing an encapsulation material in said at least one opening to adhere said
10 first microelectronic substrate core to said at least one first microelectronic device and
11 forming a first surface adjacent said microelectronic die active surface and a second
12 surface adjacent said microelectronic die back surface; and
13 forming at least one conductive via to extend from said first microelectronic
14 substrate core first to said first microelectronic substrate core second surface.

1 25. The method of claim 24, further including thermally attaching at least one
2 heat dissipation device to at least one microelectronic device back surface.

1 26. The method of claim 24, further including:
2 forming a first interconnection layer disposed proximate said first microelectronic
3 substrate core first surface, said encapsulation material first surface, and said first
4 microelectronic device active surface;

5 forming a second interconnection layer disposed proximate said first
6 microelectronic substrate core second surface, said encapsulation material second
7 surface, and said first microelectronic device back surface.

1 27. The method of claim 26, wherein forming said first interconnection layer
2 comprises:
3 forming at least one dielectric material layer on at least a portion of said first
4 microelectronic device active surface, said encapsulation material first surface, and said
5 microelectronic substrate core first surface;
6 forming at least one via through said at least one dielectric material layer to
7 expose a portion of said microelectronic device active surface; and
8 forming at least one conductive trace on said at least one dielectric material layer
9 which extends into said at least one via to electrically contact said first microelectronic
10 device active surface.

1 28. The method of claim 27, wherein forming at least one conductive trace
2 comprises forming said at least one conductive trace to extend through said at least one
3 dielectric layer to contact said at least one conductive via.

1 29. The method of claim 26, wherein forming said second interconnection
2 layer comprises:

3 forming at least one dielectric material layer on at least a portion of said first
4 microelectronic device back surface, said encapsulation material second surface, and said
5 microelectronic substrate core second surface;
6 forming at least one via through said at least one dielectric material layer; and
7 forming at least one conductive trace on said at least one dielectric material layer
8 which extends into said at least one via to electrically contact said conductive via.

1 30. The method of claim 24, further including:

2 providing a second microelectronic substrate core having a first surface and an
3 opposing second surface, said second microelectronic substrate core having at least one
4 opening defined therein extending from said second microelectronic substrate core first
5 surface to said second microelectronic substrate core second surface;

6 disposing at least one second microelectronic device within said at least one
7 opening, such that an active surface of said at least one second microelectronic device
8 resides adjacent said second microelectronic substrate core first surface and such that a
9 back surface of said at least one second microelectronic device resides adjacent said
10 second microelectronic substrate core second surface;

11 disposing an encapsulation material in said opening to adhere said second
12 microelectronic substrate core to said at least one second microelectronic device;

13 attaching said first microelectronic substrate core second surface to said second
14 microelectronic substrate core second surface; and

15 forming said at least one conductive via to extend from said first microelectronic
16 substrate core first surface to said second microelectronic substrate core first surface.

1 31. The method of claim 30, further including disposing a heat dissipation
2 device between said first microelectronic substrate core second surface and said second
3 microelectronic substrate core second surface.

1 32. The method of claim 30, further including forming at least one conductive
2 via interconnecting said first microelectronic substrate core first surface and said second
3 microelectronic substrate core first surface.

1 33. The method of claim 32, further including disposing a dielectric material
2 between said at least one conductive via and said heat dissipation device.

1 34. The method of claim 24, further including abutting said first
2 microelectronic substrate core first surface and said first microelectronic device active
3 surface against a protective film prior to disposing said encapsulation material in said at
4 least one opening.

1 35. The method of claim 34, wherein abutting said microelectronic substrate
2 core first surface and said at least one microelectronic device active surface against a
3 protective film comprises abutting said first microelectronic substrate core first surface

4 and said first microelectronic device active surface against an adhesive layer on said
5 protective film prior to disposing said encapsulation material in said at least one opening.

1 36. A method of fabricating a microelectronic substrate, comprising:

2 providing a first microelectronic substrate core having a first surface and an
3 opposing second surface, said first microelectronic substrate core having at least one
4 opening defined therein extending from said first microelectronic substrate core first
5 surface to said first microelectronic substrate core second surface;

6 disposing at least one first microelectronic device having an active surface and a
7 back surface within said at least one opening such that said first microelectronic device
8 active surface resides adjacent said first microelectronic substrate core first surface;

9 disposing a first encapsulation material in said microelectronic substrate core
10 opening adhering said first microelectronic substrate core to said at least one first
11 microelectronic device, forming a first surface adjacent said first microelectronic die
12 active surface and a second surface adjacent said first microelectronic die back surface;

13 providing a second microelectronic substrate core having a first surface and an
14 opposing second surface, said second microelectronic substrate core having at least one
15 opening defined therein extending from said second microelectronic substrate core first
16 surface to said second microelectronic substrate core second surface;

17 disposing at least one second microelectronic device having an active surface and
18 a back surface within said at least one opening such that said second microelectronic

19 device active surface resides adjacent said second microelectronic substrate core first
20 surface;
21 disposing a second encapsulation material in said second microelectronic core
22 opening adhering said second microelectronic substrate core to said at least one second
23 microelectronic device, forming a first surface adjacent said second microelectronic
24 active surface and a second surface adjacent said microelectronic die back surface; and
25 attaching said first microelectronic core to said second microelectronic core such
26 that said first microelectronic device active surface oriented to face said second
27 microelectronic device active surface.

1 37. The method of claim 36, further including forming an interconnection
2 layer disposed proximate said first microelectronic substrate core first surface, said first
3 encapsulation material first surface, and said first microelectronic device active surface
4 and further including forming a second interconnection layer disposed proximate said
5 second microelectronic substrate core first surface, said second encapsulation material
6 first surface, and said first microelectronic device active surface; and wherein said
7 attaching said first microelectronic core to said second microelectronic core includes
8 forming electrical connections between said first and second interconnection layers.

1 38. The method of claim 36, further including forming an interconnection
2 layer disposed proximate at least one of said first microelectronic substrate core second
3 surface, said first encapsulation material second surface, and said first microelectronic

4 device back surface, and said second microelectronic substrate core second surface, said
5 second encapsulation material second surface, and said second microelectronic device
6 back surface.

1 39. The method of claim 36, further including forming at least one conductive
2 via to extend from said first microelectronic substrate core first surface and said first
3 microelectronic substrate core second surface.

1 40. The method of claim 36, further forming including at least one conductive
2 via to extend from said second microelectronic substrate core first surface and said
3 second microelectronic substrate core second surface.

1 41. The method of claim 36, further including forming at least one conductive
2 via interconnecting said first microelectronic substrate core second surface and said
3 second microelectronic substrate core second surface.

1 42. The method of claim 36, further including thermally attaching at least one
2 heat dissipation device to at least one of said at least one first microelectronic device back
3 surface and said at least one second microelectronic device back surface.

1 43. The method of claim 42, further including forming at least one conductive
2 via interconnecting said first microelectronic substrate core first surface and said second
3 microelectronic substrate core first surface.

1 44. The method of claim 43, further including disposing a dielectric material
2 between said at least one conductive via and said heat dissipation device..